

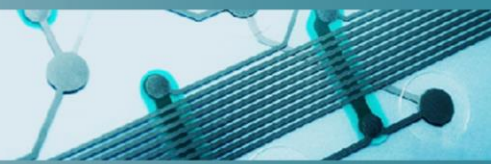
A Multek White Paper
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Extracting Modal Resonance Effects From TDR Measurements



MULTEK

One-stop Interconnect Solutions Provider



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EXECUTIVE SUMMARY

If we tap a tuning fork, part of the energy from the tap will get transferred to the tuning fork. This transferred energy causes the tuning fork to oscillate. At the beginning, the amplitude of the oscillations will be strong. But with each back-and-forth oscillation, part of the energy in the tuning fork will dissipate into the surrounding air, causing the amplitude of the oscillations to decrease with time.

Conceptually an impulse (the tap) excites a structure resonance (the tuning fork), causing it to oscillate. Depending on the size of the tuning fork, the frequency at which it oscillates will vary. Longer tuning forks oscillate at a lower frequency, while shorter tuning forks will oscillate at a higher frequency.

A similar situation can occur in a PCB interconnect, when the leading edge of a TDR (Time Domain Reflectometer) pulse excites a structure resonance in the PCB. And like the tuning fork example, different length structures inside a PCB interconnect will oscillate at different frequencies. For example, via stubs and via through structures are physically small, so they will oscillate at a relatively high frequency. Long traces, on the other hand, are physically large, so they will oscillate at relatively low frequencies.

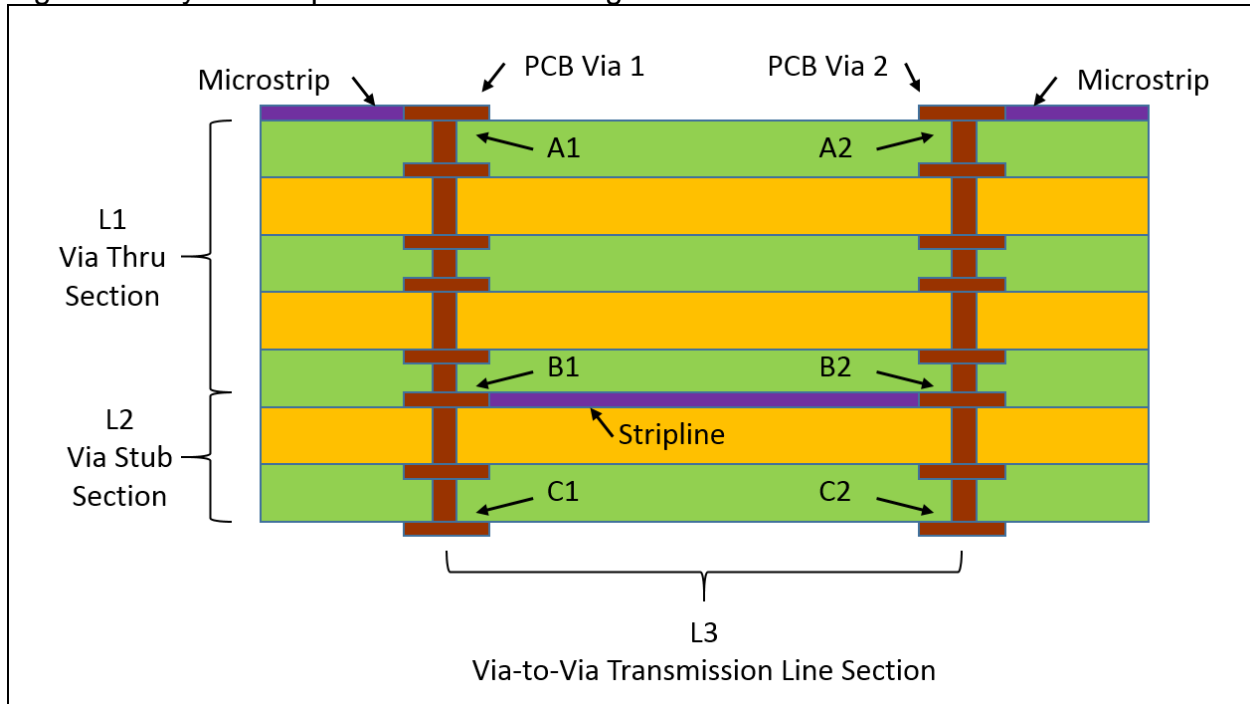
Because the basis of a TDR is an oscilloscope, it will also capture these oscillations, superimposing them on reflections from impedance mismatches that are also present inside the PCB interconnect. If the end goal of the TDR measurement is to quantify the interconnect's impedance mismatches, then these superimposed oscillatory waveforms must first be removed from the TDR measurements.

This white paper describes PCB interconnect resonances in greater detail and shows a method by which they can be properly identified and removed from the TDR measurements.

Interconnect Impedance Mismatches

Referring to Figure 1, a typical single ended PCB interconnect can include microstrip transmission line segments on the outer layers of the PCB, stripline transmission line segments on an inner layer of a PCB and via structures that electrically connect the microstrip and stripline sections together.

Figure 1: Physical Representation of a Single Ended PCB Interconnect



At the points where the microstrip and stripline attach to the via (A1, A2, B1 and B2 in Figure 1) an impedance mismatch will occur because the cross section of the interconnect changes (between rectangular traces and circular vias) and the direction changes (between traces parallel to the dielectric layers and vias perpendicular to the dielectric layers). In addition, if the PCB interconnects have via stub sections, then an impedance mismatch will also occur at the end of the stub (C1 and C2 in Figure 1).

Whenever a signal that propagates through an interconnect encounters an impedance mismatch, part of the signal gets reflected back towards the source it originally came from. In Figure 1, such impedance mismatch reflections occur at A1, A2, B1, B2, C1 and C2.

Assume for the moment that a single fast rise time digital pulse is propagating through the structure shown in Figure 1 from left to right, and that the focus will be on the leading edge of this digital pulse. At location A1, a portion of this digital pulse's leading edge will get reflected back towards the source. The remainder then proceeds down through the via towards location B1. At B1 the leading edge again encounters an

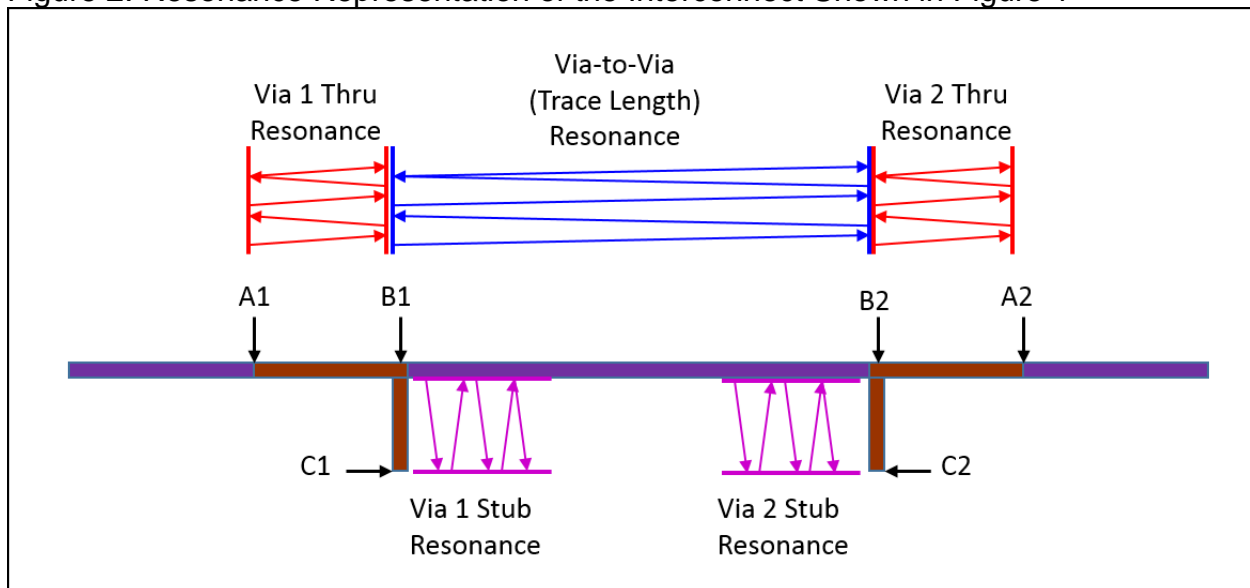
impedance mismatch, so another portion gets reflected back towards the source. But when this second reflection arrives at A1, it again sees the A1 impedance mismatch, in which case a portion of the reflected signal gets reflected back towards B1. This process repeats until all the energy in the reflections trapped between A1 and B1 manage to escape either back toward the source on the left side of A1 or forward towards the output on the right side of B1.

The via through section located between A1 and B1 traps not only the leading edge of a single digital pulse, but also its trailing edge and repeats this for every other digital pulse that passes through this interconnect. This introduces large amounts of distortion because the energy trapped from the previous digital pulse gets mixed up with the energy from the current digital pulse creating a form of signal distortion called Inter Symbol Interference (ISI).¹ As one can well imagine, if the time it takes to dissipate the trapped energy is longer than the time it takes for a digital pulse to propagate through the interconnect, then reflections from multiple prior symbols (digital bits) can mix with the current symbol (digital bit) that is propagating through the interconnect.

Structure Resonances

The energy that bounces back and forth between the impedance mismatches located at A1 and B1 is analogous to the tongs in a tuning fork bouncing back and forth between their extreme positions. And like the tuning fork, the inverse of the time for each “bouncing back and forth” oscillation is equal to the structure’s resonant frequency.

Figure 2: Resonance Representation of the Interconnect Shown in Figure 1



Because there are multiple impedance mismatches in the interconnect shown in Figure 1, multiple resonance structures are created. Referring to Figure 2, besides the resonant structure between A1 and B1 (via 1 thru resonance), the interconnect also has

¹ In a digital pulse stream, each digital pulse associated with either a logical 0 or logical 1 is called a symbol.

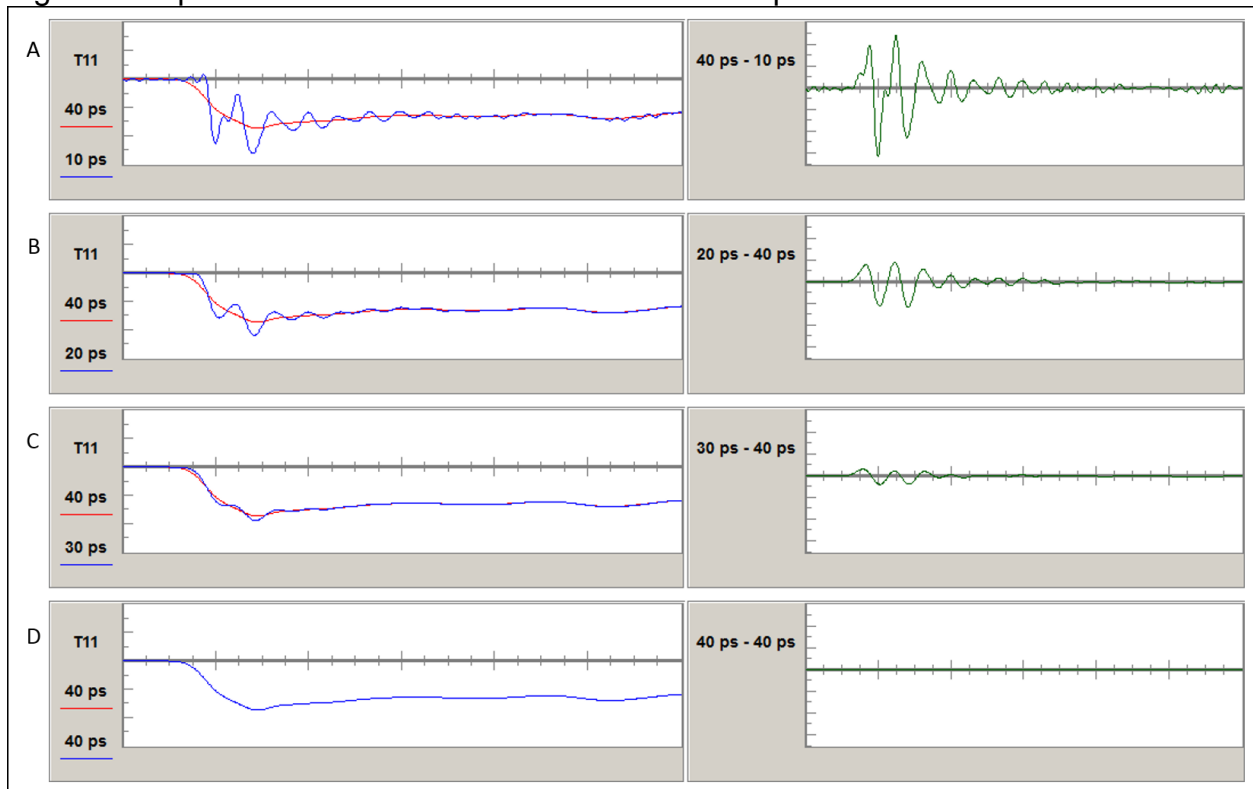
resonant structures created by impedance mismatches B1 and C1 (via 1 stub resonance), B1 and B2 (via-to-via trace resonance), B2 and C2 (via 2 stub resonance), and B2 and A2 (via 2 thru resonance).²

Note that removing the via stubs (B1 – C1 and B2 – C2), using, for example, backdrilling, does not eliminate all resonant structures in this interconnect. Indeed, at very high data rates, even after the via stubs are removed, the remaining non-via stub resonances can continue to introduce significant amounts of signal distortion.

An Example of a Via Resonance Excited by the Leading Edge of a TDR Pulse

Figure 3 shows a series of responses when TDR pulses having different rise times excite a via thru resonance. The top left graph (blue trace) is the T11 REFL (reflect) response for a TDR pulse having a rise time of 10 ps.³ The graphs below are for TDR pulses having rise times of 20 ps, 30 ps and 40 ps respectively. For reference, each graph also contains the response of the 40 ps TDR pulse (red curves). The corresponding graphs on the right side of Figure 3 (green curves) show the difference between the left curves and the 40 ps TDR pulse.

Figure 3: Impact of TDR Rise Time on Resonance Amplitude



Referring to the left graphs in Figure 3, one can see that as the rise time of the TDR is increased, the amplitude of the resonance decreases. Also note from the right graphs

² Secondary resonant structures can also exist between A1 and B2, A1 and C1, etc.

³ See the white paper, "Two Domains. Four Kinds of Ratios" for a detailed description of a REFL response.

that the resonant frequency does not change with rise time – since it is dependent on the structure, not the signal energy that is trapped in it, just as a tuning fork frequency does not change with how strongly it is struck.

From the curves in Figure 3, one can see that TDR rise time can have a significant impact on the amplitude of these structural resonances that get superimposed on top of any characteristic impedance measurements associated with any controlled impedance transmission lines that exist within the interconnect.

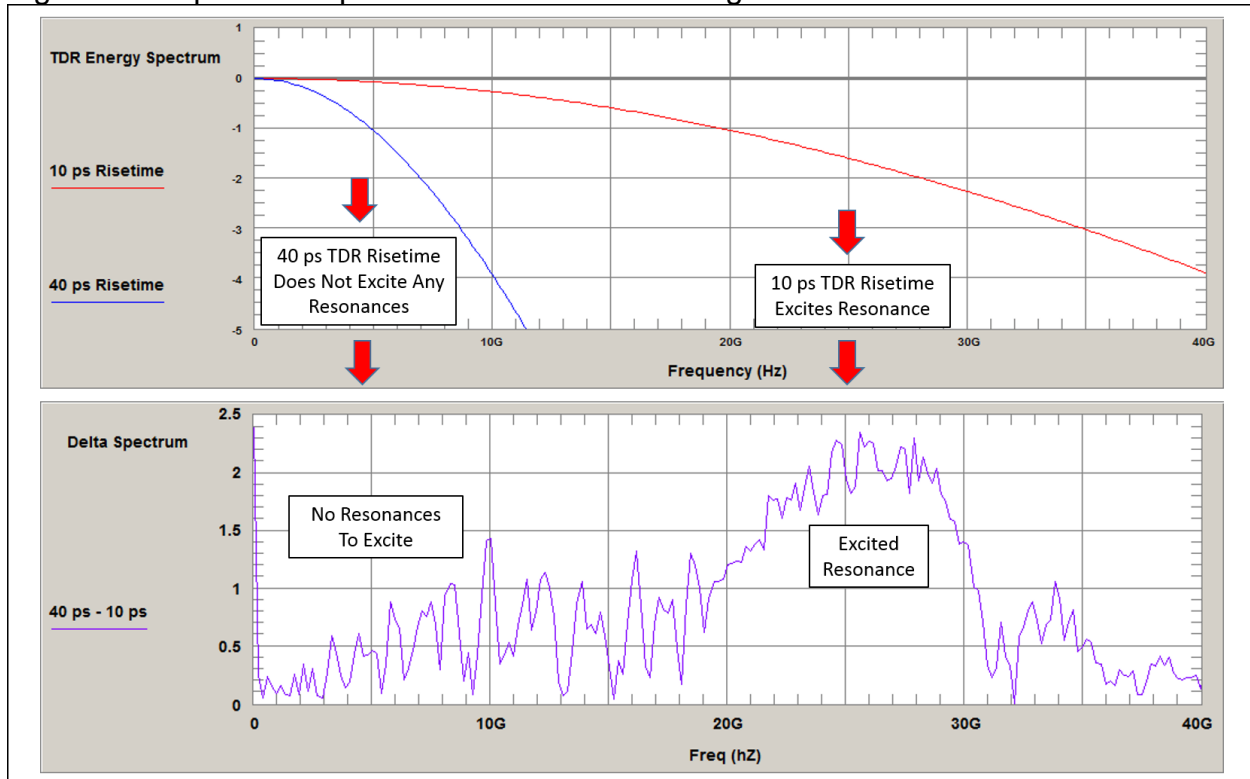
Spectral Representation of a Via Through Resonance

The physical mechanism for why faster rise times result in higher amplitude resonances can be better understood if analyzed in the frequency domain. The energy spectrum of a TDR pulse, can be approximated by the formula

$$BW = 0.35 / t_r \tag{1}$$

where t_r is the rise time of the TDR. This inverse relationship states that as the rise time of the TDR decreases, the amount of energy contained in the TDR pulse at higher frequencies increases. Thus a 10 ps rise time TDR pulse contains significantly more energy at higher frequencies than a 40 ps rise time TDR.

Figure 4: A Spectral Representation of a Via Through Resonance



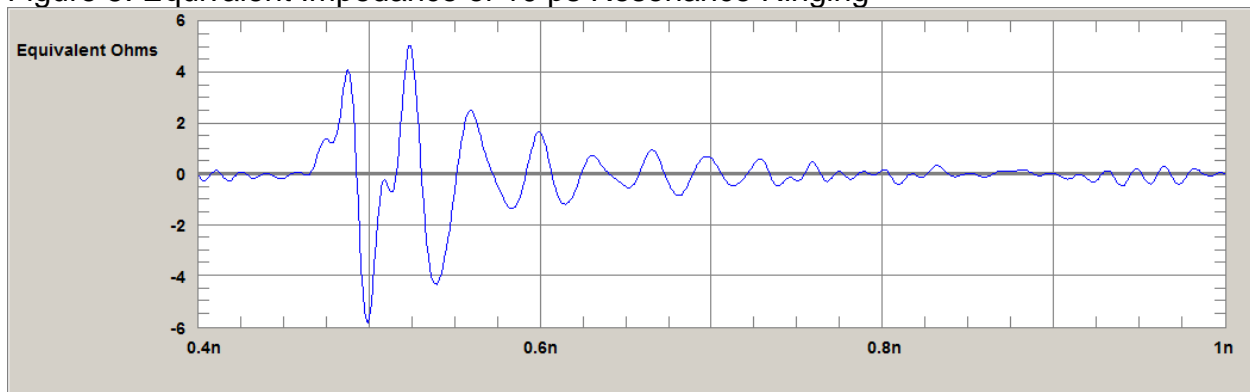
If there is no spectral energy in the TDR at the resonant frequency of the PCB structure, then the structure does not get excited, and no ringing occurs. For the case shown in Figure 3, the 10 ps TDR pulse contains enough high frequency energy to excite the via thru resonance at 25 GHz, while the slower 40 ps TDR pulse does not.

In the top graph of Figure 4, the energy spectrums of 10 ps and 40 ps rise time TDR pulses are plotted as a function of frequency. The bottom graph of Figure 4 is the spectrum of the via thru resonance associated with the top right graph of Figure 3. Comparing the two graphs in Figure 4, one can readily see that the 40 ps rise time TDR does not contain enough energy at 25 GHz to excite the resonant frequency of the via thru resonance. The 10 ps TDR, on the other hand, has ample spectral energy at this frequency. This correlates very well with the top and bottom middle graphs of Figure 3, where the via thru ringing is quite pronounced when excited by the 10 ps TDR pulse, but is almost completely non-existent when excited by the 40 ps TDR pulse.

This resonance amplitude dependence on TDR rise time can create problems when the TDR responses of different rise time TDRs are compared. For example, the standard TDR normally used in a PCB manufacturing environment only has a very slow 170 ps rise time. Most TDRs used in a product development environment have rise times on the order of 30 ps or faster.

If the interconnect being characterized contains resonant structures that are excited by the 30 ps or faster rise time TDRs, and not by the slower 170 ps PCB production TDRs, then the two measurements will not correlate. The 30 ps or faster TDR will contain a significant amount of resonant “ringing” superimposed on the characteristic impedance that the 170 ps TDR will not display. This superimposed ringing can cause the measured TDR response to falsely indicate the characteristic impedance of any transmission line segments located after the resonant structure exceeds the design specification.

Figure 5: Equivalent Impedance of 10 ps Resonance Ringing



This is shown in Figure 5, which plots the residual T11 ringing ratio of the upper right graph in Figure 3 converted into ohms using the following standard T11 to characteristic impedance formula

$$Z_0 = 50g(1+T_{11}) / (1-T_{11}) \quad (2)$$

From Figure 5 one can see that if the resonant ringing is falsely included in the calculation of the characteristic impedance using equation (2), then the error in ohms can be as high as 5 to 6 ohms, which is equivalent to the entire +/- design tolerance typically allocated for a 50 single ended transmission line.

Factors Impacting the Selection of the Optimum Measurement Rise Time

The presence of structural resonances complicates the problem of selecting an optimum rise time. If one wants to only characterize the characteristic impedance of any transmission line segments immediately following any resonant structures, then the data presented herein implies a slower rise time is preferred over a faster rise time.

A complete “end-to-end” characterization of the entire interconnect - necessary to capture all distortion producing artifacts present in the interconnect including not only variation in characteristic impedance but also resonances associated with any thru and stub via structures included in the total interconnect – requires a very fast TDR rise time pulse. However, if the TDR rise time is much faster than the rise time of the actual signal, then it can excite resonant structures that the slower rise time of the actual signal will not excite. In this case, the TDR will record distortion-producing resonances that the actual signal will not excite.

A third approach resides in between the two just described. Recall that the ringing amplitudes of the resonance structures vary as a function of the rise time. Using a TDR rise time faster than the signal will introduce ringing amplitudes higher than what the actual circuit will experience. Conversely, if the TDR rise time is much slower than the rise time of the signal, then it will not record resonances that introduce signal distortions during actual operation.

From this one can conclude that the optimum characterization of the total interconnect should be made with the TDR rise time set to the same rise time as the signal that will pass through the interconnect during actual operation.⁴

What if One Only Wants to Measure the Characteristic Impedance?

There are several options one can use to isolate the characteristic impedance from the ringing that these resonant structures introduce into the TDR measurement. For example:

⁴ In many products, it is possible to increase the data rate (frequency) of the signal that passes through a PCB interconnect by simply changing the clock frequency or the chip set that is connected to the interconnect. In such a situation, it is often desirable to design the interconnect for a data rate that is not yet practical - in essence incorporating growth into the PCB design. In such situations, it is desirable to decrease the TDR's rise time to match the faster rise time of the future signal, rather than match the rise time of the current signal. This is one of the reasons why many TDR instruments used in R&D and product design laboratories have the option of changing the rise time. The problem occurs when the rise time of such a programmable TDR is set to its fastest rise time (faster is always better), and in the process, it will record resonances that even future speed upgrades will never excite.

1. Remove non-optimized via structures (or other interconnect structures) that create resonances in the interconnect being characterized. This, of course is not possible if actual interconnects that contain non-optimized via structures are being characterized.
2. Ignore the characteristic impedance of the portion of a transmission line immediately following the resonant structure, preferring instead to only measure that portion that spatially occurs after the ringing has attenuated to an acceptably low level. Note that in some cases, this option is not practical. For example, attempting to characterize a short length of transmission line immediately following a resonant structure that rings for a period of time longer than the propagation delay down the transmission line. In such a case, the only solution is to revert back to option 1 above.
3. Apply the technique outlined in this paper, where two or more sets of measurements are made using different rise times, and then comparing a lower rise time measurement with a faster rise time measurement.
4. And finally, instead of attempting to characterize the transmission line segments of a complex interconnect on an actual product that includes multiple resonant structures, add/measure a simple interconnect consisting of a length of transmission line that is spatially longer than any ringing introduced by the via launch structure. Then only measure the portion of the transmission line that is spatially beyond the ringing.

Option 4 is the typical structure that already exists on impedance coupons added to a production panel to confirm layers containing controlled impedance interconnects are properly constructed. This option, however, does not fully resolve the characterization problem because many production TDRs still have rise times that are much slower than the actual rise times of the signals propagating through the interconnect. This slower rise time has the effect of spatially averaging the variations along a transmission line, something that the actual signal that passes through the interconnect does not do. So while the coupon concept still has value when characterizing high performance interconnects, it is the slow rise time TDRs that are preventing absolute (non-averaged) characterizations from being made.

For example, a typical production TDR has an approximate rise time of around 170 ps. Several of the most popular TDR instruments currently used in R&D and development laboratories have rise times of 24 ps – which slow down to approximately 30 – 40 ps when a test cable is attached.⁵ The next generation of TDRs have rise times approaching 10 to 30 ps.⁶

In this environment, improving the launch structure of existing coupon designs to minimize via-induced resonances, and then measuring absolute (rather than average)

⁵ Tektronix SD-24 and 80E04, and Agilent/Keysight Technologies 54754.

⁶ Tektronix 80E08B and 80E10B, and Keysight Technologies N1055A.

characteristic impedance using a faster rise time TDR (and compatible probe) is a more rational approach to de-embedding (separating) structure resonance effects from characteristic impedance that are inherently combined into one TDR measurement.

Characterizing a complex interconnect on an actual PCB – containing not only controlled impedance transmission line segments, but also multiple resonant structure – using a 10 ps TDR almost always excites resonances that interfere with the proper characterization of the transmission line segments of the interconnect.

Conclusions

Complete characterization of high performance interconnects requires faster rise time TDRs. However, fast rise time TDRs not only measure characteristic impedance of PCB transmission lines, but also ringing from structural resonances embedded in the interconnect being measured. These superimposed resonances can cause the measured TDR response to falsely indicate the characteristic impedance of any transmission line segments located directly after the resonant structure exceeds the design specification. The ringing from these structural resonances must be de-embedded (removed) from the TDR measurements before the characteristic impedance can be calculated.

Faster rise time TDRs also more accurately characterize absolute characteristic impedance than slower rise time TDRs –which spatially average the characteristic impedance. At higher data rates (frequencies), absolute characteristic impedance is more representative of how much distortion a controlled impedance transmission line introduces than the average characteristic impedance.

About the Author:

Franz Gisin is Director of Signal Integrity at Multek's Interconnect Technology Center in Milpitas, California. Franz Gisin's core focus is the electrical characterization of PCB-based high performance digital, RF and microwave interconnects.

Prior to Multek, Franz Gisin has worked for over 40 years in electromagnetics including EMC (Electromagnetic Compatibility), signal integrity and the characterization and modeling of high performance interconnects.

Franz Gisin has a BS in Electrical Engineering and an MS in Applied Mathematics.

About Multek's Interconnect Technology Center (ITC):

The Interconnect Technology Center (ITC) is Multek's advanced technology development organization. we engage with customers early in the design process to create innovative solutions to pressing technical challenges. Our technical core competencies are aligned to meet the challenges of trends around increasing data rates, increasing density of PCBs, and new shape requirements.



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