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TDR Measurements of PCB Interconnect Artifacts

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EXECUTIVE SUMMARY

TDR (Time Domain Reflectometer) measurements of actual PCB (Printed Circuit Board interconnects often do not correlate well with those made on coupon transmission lines co-located on the same panel as the actual PCB.

One of the reasons for this difference is due to the inclusion of non-transmission line structures in PCB interconnects that are not present in coupon transmission lines.

This white paper describes how these non-transmission line structures introduce artifacts in the TDR measurements that should not be misinterpreted as variations in the characteristic impedance of the transmission line portions of the PCB interconnect.[1]

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[1] A PCB interconnect includes everything between the point where the signal is first injected into the PCB and if applicable, the point where the signal is extracted from the PCB. For example, component and connector attachment pads, vias, transmission lines, test points, trace bends, routing traces through via fields, serpentine and trombone style delay lines and macro geometries such as parallel buss structures.

Background

It is customary in a PCB manufacturing facility to confirm controlled impedance interconnects on high performance PCBs are properly constructed by using a TDR instrument to measure coupons that contain controlled impedance transmission lines whose physical dimensions are identical to what was specified for use in the PCB interconnects. These coupons are typically located in unused areas of a panel, for example along the periphery of the panel or sandwiched between PCBs in unused areas of the panel. The premise is that if the TDR measurements of the transmission lines on the coupon meet the design specifications, then impedance controlled interconnects on the PCB will also meet the design specification.

To confirm this premise is valid, TDR measurements are sometimes made on actual PCB interconnects that contain controlled impedance transmission lines. However, the measurements of the PCB interconnect does not always correlate well with the coupon measurements because the PCB interconnect contains non-transmission structures that are not properly processed by the TDR's post measurement software used to convert the raw TDR measurements into characteristic impedance.

What a TDR Actually Measures

In order to understand how non-transmission line structures impact TDR measurements, one must understand what additional kinds of structures TDRs can measure beside the characteristic impedance of transmission lines.

The sensor at the heart of a TDR is an oscilloscope that measures voltage as a function of time. By combining this oscilloscope with a constant voltage pulse generator and a precision impedance (usually 50 ohms), this sensor can measure the sum of two voltages, $V_{\mathrm{OUT}} + V_{\mathrm{REFL}}$, where V_{OUT} is the voltage of the pulse that is "sent out" of the TDR, and V_{REFL} is the voltage that gets "reflected back into" the TDR from whatever structure is connected to the TDR. Because V_{OUT} is known, one can easily obtain V_{REFL} by subtracting V_{OUT} from the sensor measurements, and then divide the two separated values to obtain the reflection coefficient, $T_{11} = V_{\mathrm{REFL}} / V_{\mathrm{OUT}}$.[2]

Since the precision resistance inside the TDR is also known (the 50 ohms), it is possible to convert the reflection coefficient into a variety of impedance parameters, depending on what is attached to the TDR terminals. For example, one can connect a uniform transmission line to the TDR, in which case the reflection coefficient can be converted into its characteristic impedance, Z_0, using the formula,

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[2] In the literature, ρ is also a commonly used symbol for T_{11}. The frequency domain equivalent of T_{11}, measured with a VNA (Vector Network Analyzer), is the S_{11} ratio. Γ is also a commonly used symbol for S_{11}.

$$Z_0 = 50g(1+T_{11})/(1-T_{11}) \quad (1)$$

However, if one inserts a non-transmission line structure somewhere inside a uniform transmission line, then equation (1) can no longer be used to calculate the “impedance” of that non-transmission line structure.

Many of these non-transmission line structures (which will be described in greater detail in the next section) can be modeled as either a discrete shunt capacitance, C , or a discrete series inductor, L . If the structure behaves like a discrete shunt capacitance, then it will show up in the TDR measurements as a negative “dip”. If the structure behaves like a discrete series inductor, it will show up in the TDR measurement as a positive “peak”.

The area of the dip or peak can be used to find the capacitance and/or inductance of the non-transmission line structure. Once these are found, one can compute the impedance using the following two formulas.

$$Z_L = j2\pi f L \quad (2)$$

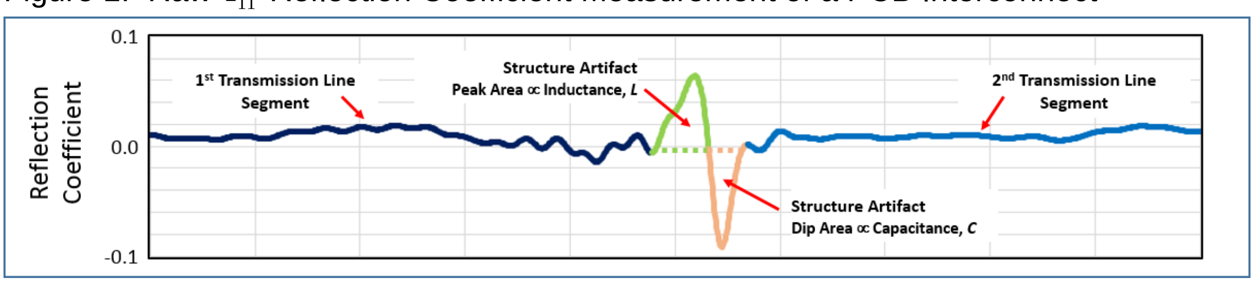
$$Z_C = 1/(j2\pi f C) \quad (3)$$

Note that equations (2) and (3) are not the same as equation (1) used to find the characteristic impedance of a uniform controlled impedance transmission line. Many TDR instruments do not have the capability to automatically locate the dips and peaks in a measurement that are associated with non-transmission line structures, or calculate their respective impedances per equations (2) and (3). This can pose a problem if such a TDR is used to characterize a PCB interconnect that contains non-transmission line structures. More sophisticated laboratory-grade TDR instruments sometimes have optional software that can be added to the instrument that can calculate the capacitances and inductances of non-transmission line structures. But even with such a setup, one must still manually identify which locations along the TDR measurement are due to non-transmission line structures.

An Example of a Non-Uniform Transmission Line Interconnect

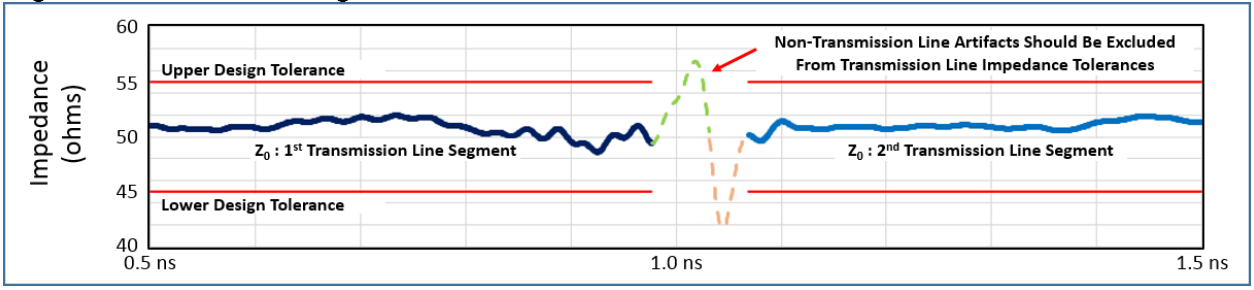
Figure 1 is the raw reflection coefficient T_{11} measurement of a section of PCB interconnect that contains two non-transmission line structures.

Figure 1: Raw T_{11} Reflection Coefficient Measurement of a PCB Interconnect



Notice that this structure contains both a series inductance (the peak) and a shunt capacitance (the dip) sandwiched between two controlled impedance transmission line segments.

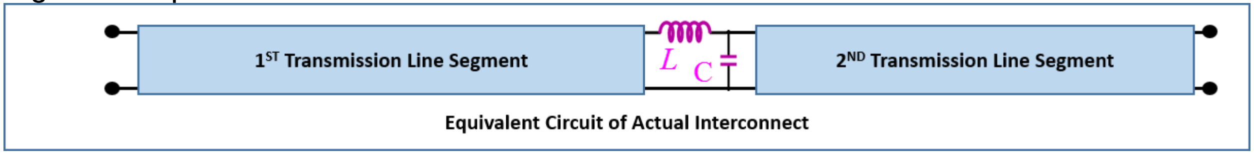
Figure 2: De-Embedding Structure from PCB Interconnect



Referring to Figure 2, one can de-embed (extract) the left and right transmission line segments from the PCB interconnect and apply equation (1) to calculate their characteristic impedances and ascertain whether they fall between any applicable design tolerance limits. However, it is not correct to apply equation (1) to the peak and dip associated with the non-transmission line structure. Nor is it appropriate to apply any upper and/or lower design tolerance limits meant for the controlled impedance transmission line segments of the PCB interconnect.

Figure 3 shows the equivalent circuit of this section of the PCB interconnect. Notice that it cannot be modeled as a continuous transmission line.

Figure 3: Equivalent Circuit of the PCB Interconnect



While the non-transmission line structure in this example contains both a fairly large series inductance and shunt capacitance, many actual non-transmission line structures contain only one or the other, and have inductances and capacitances that are not as high. As a result the magnitudes of the structure's peaks and dips are not that large. If the characteristic impedance of the transmission line segments on either side of such a structure are close to the nominal design value, then also applying equation (1) to the peaks and dips associated with these non-transmission line structures will result in an "apparent" characteristic impedance that is still within the specified tolerance limits.

However, if the nominal characteristic impedance of the transmission line segments are close to either of the upper or lower design limits, then the peak or dip can erroneously cause the "apparent" characteristic impedance to exceed the limit, resulting in an incorrect failure.

From this simple example, one can see that a complex interconnect consisting of one or more capacitive and inductive structures sandwiched between several transmission line segments can result in a fairly complex TDR waveform that contains more than just the characteristic impedance of the transmission line segments of the interconnect.[3]

Some Examples of Non-Transmission Line Structures

Figure 4 shows a typical single ended and differential pair transmission line on a controlled impedance coupon. Both of these transmission lines are straight and uniform along their entire lengths.

Figure 4: Typical Coupon Transmission Line Constructions

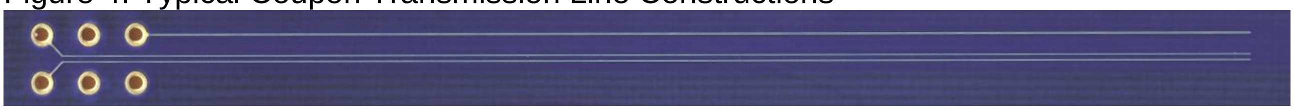
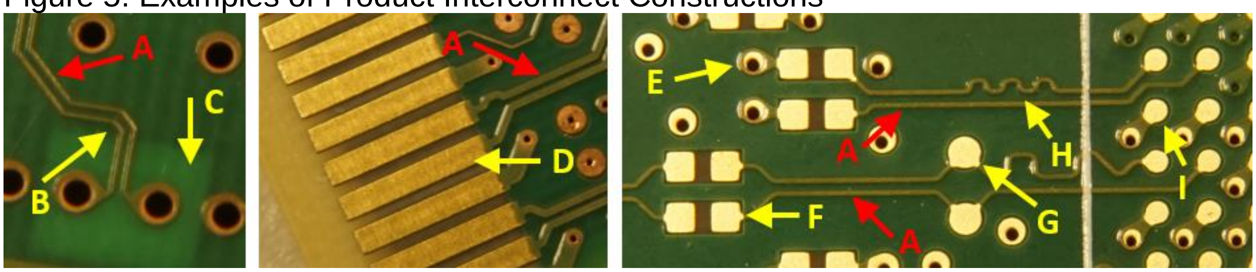


Figure 5 shows some typical examples of interconnects on actual product. Notice that these interconnects are considerably more complex than the coupon transmission lines shown in Figure 4.

Figure 5: Examples of Product Interconnect Constructions



Referring to Figure 5, the controlled impedance transmission lines segments are identified by the letter A. Non-controlled impedance structures sandwiched between these transmission line segments include bends (B), large antipads (C), card edge connectors (D), in circuit vias (E), discrete component pads (F), test pads (G), skew control structures (H), and vias in via fields placed in close proximity to the transmission lines (I).

These non-transmission line structures introduce lumped element series inductors or shunt capacitors into the interconnect that must be removed from the TDR measurements using the de-embedding method described in the previous section, before a determination of whether the transmission line segments of the interconnect conform to specified design tolerances.

The inclusion of these non-transmission line structures in an actual PCB interconnect can present formidable problems when it comes to determining if the transmission line

[3] Although not addressed in this white paper, a TDR instrument can also measure damped oscillatory waveforms from structures that resonate when excited by the rising edge of the TDR pulse.

sections of the interconnect meet specified design constraints. As noted earlier, a TDR is not able to determine if the variations in the measurements are due to variations in the characteristic impedance of the transmission line segments or the shunt capacitances and series inductances associated with non-transmission line structures. So a manual step must be inserted into the measurement process to isolate where along the TDR measurement the transmission line segments are located if the measurement software of TDR instruments is not sophisticated enough to divide the measurement into multiple sections of pass fail limits that just overlap the transmission line portions of the interconnect.

A Practical Solution

If a measurement of a transmission line structure on an actual product is necessary, it makes a lot of practical sense to add a simple straight line transmission line structure similar to those on the coupons to the product, rather than attempt to measure an existing complex interconnect containing both transmission line segments and non-transmission line segments.

Conclusions

TDR measurements of interconnects on actual product that contain both controlled impedance transmission line segments and non-transmission line structures can make the interpretation of TDR measurements difficult. This is because isolating those portions of the TDR waveform corresponding to controlled impedance transmission line sections from non-transmission line capacitive and inductive structures such a vias and test pads requires a prior knowledge of the design of the interconnect and the capability to correlate these structures to specific temporal locations along the TDR measurement curve.

Because of these complexities, it is often more practical to measure a simple straight line controlled impedance transmission line structure that is added to the PCB.

<u>**About the Author:**</u>
Franz Gisin is Director of Signal Integrity at Multek's Interconnect Technologhy Center in Milpitas, California. Franz Gisin's core focus is the electrical characterization of PCB-based high performance digital, RF and microwave interconnects.

Prior to Multek, Franz Gisin has worked for over 40 years in electromagnetics including EMC (Electromagnetic Compatibility), signal integrity and the characterization and modeling of high performance interconnects.

Franz Gisin has a BS in Electrical Engineering and an MS in Applied Mathematics.

About Multek's Interconnect Technology Center (ITC):
The Interconnect Technology Center (ITC) is Multek's advanced technology development organization. we engage with customers early in the design process to create innovative solutions to pressing technical challenges. Our technical core competencies are aligned to meet the challenges of trends around increasing data rates, increasing density of PCBs, and new shape requirements.

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