High-Density Interconnects: Enabling the Intelligence of Things

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Abstract

The rapid evolution of high-density interconnects printed circuit board (HDI PCB) technologies over the last five years has been accelerated largely by the mass production demands for global deployment of 3G and 4G mobile phone products at attractive consumer pricing. The major capacity expansions in Asia factories has allowed circuit shipments at the highest volumes and quality levels yet experienced since the invention of the circuit board in the 1950s.

As the Internet of Things (IoT) spawns new intelligent connected platforms (IP) for sensing and control products such as wearable electronics, home automation, and medical monitoring, HDI processing is being applied to rigid-flexible printed circuits (RFPC) and multilayer flexible printed circuits (FPCs), modified in new ways to achieve mechanical, physical, and chemical exposure robustness and low latency communication to the cloud. The purpose of this article is to explore the key requirements and new approaches required for the application of HDI, especially stacked, copper filled microvia processing of thinner, low loss materials, to achieve the routing and solder joining capabilities required by advanced surface mount technology and final assembly techniques dictated for

leading edge semiconductor component packaging densities.

Background

Beginning in the 1980s, the electronics industry began the early days of transition from pin-in-hole wave soldering to surface mounting of increasingly complex semiconductor packages. Strategic technical analysts at companies such as IBM, Bell Labs (Western Electric), Digital Equipment, Hitachi, NEC, and Hewlett Packard realized the existing PCB processes and materials faced an impending industry-wide capability bottleneck with urgent implications in limiting copper trace and solder pad featuring. From this exigency came the industry-wide invention of a continuing variety of microvia processes and production systems that continues to this day. Today, the copper filled, stacked laser drilled microvia multilayer process is the dominant in global production.

In a parallel but separate roadmap, the flexible circuit has evolved since its inception as an early alternative to cabling and power distribution. Flexible printed circuits evolved quickly in the early 1980s to become the dominant form factor for very fine-pitch semiconductor packaging substrates and liquid crystal display interconnection. With reel-to-reel mass production lines adapted for wet chemical and fine-line lithographic techniques, FPCs continue to be an essential element in product design solutions today, especially for touch screen and large area LCD and LED based displays.

The HDI-FPC hybrid platform, known as rigid-flex or RFPCs, has been adapted to a number of different stackups to solve designers' interconnect-product structuring challenges, resulting in an extensive patent literature of innovation. In general, one or more fine line single or double sided FPCs are applied as the conformal connection planes in a stackup combining HDI rigid PCB inner and outer layers, and appropriate adhesives and coverlays to both combine and protect the core for laser via creation, as well as final plated through-hole (PTH) and final metal finish plating steps. HDI layers and sub-composites with laser drilled vias combined with stacked, copper filled vias up to 16 layers has become the state of the art in circuit design for the newest generation of mobile phones, wearable electronics, and IoT modules.

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High-Density Interconnect Stackup Basics

The increasing need for greater functionality in a small form factor drives the HDI PCB stackup designs.

The interconnect structures in HDI PCB include buried vias and microvias. In standard HDI, such as a 1+N+1 and an i+N+i stack up, both buried vias and microvias are used. Every layer interconnect connection (ELIC) uses only stacked copper filled microvias. Each of these stackup structures enable designs for smart, connected devices and the choice of HDI structures is dependent upon several factors including functionality, connectivity, product dimensions, weight, reliability, assembly requirements and user experience.

Table 1 provides a high-level definition and comparison of the HDI Stackup structures.

Buried vias may be drilled into just one internal core that connects the top and bottom layer or into a multi-layer subpart. These buried vias connect multiple layers together internally using standard through-hole requirements for annular ring, aspect ratio and drill to copper requirements.

Stacked microvias are just as it states. The vias are laser drilled one on top of the other in adjacent layers creating a stack of microvias in the PCB. For best reliability, it is recommended that only copper filled microvias be used when stacking. Stacked microvia can be combined with buried and thru-hole technology (Figure 1).

Staggered microvias are laser drilled offset to the other microvia in adjacent layers creating a staggering pattern of microvias between layers in the PCB. The microvias do not necessarily need to be copper filled and are often resin filled from the adjacent dielectric layer. Staggered microvia can be combined with buried and thru hole technology (Figure 2).

Every layer interconnect connection (ELIC) allows for dynamic connection between any two layers within the circuit layout. This flexibility optimizes useable area for dense component placement and provides a higher level of circuit density for complex routing challenges. ELIC employs a method of using stacked microvias on every layer. This process starts with an ultra-thin core that has microvias drilled and solid copper filled as the base. Using this initial core, a sequential lamination is use to add additional dielectric layers with laser drilling and copper via filling as required on both sides to achieve the final stackup (Figure 3).

This allows for the unique process of starting and ending any routing requirement on any layer and opens routing channels and provides the ability to reduce the overall thickness of the PCB. ELIC design guidelines follow the same structures as for stacked microvia, but provide higher internal routing density due to the elimination of buried through-hole vias in the initial sub buildup, and eliminating holes

Stack Up Structure Designation	Define	Structured
1+N+1	High-density routing on top and bottom layers only.	**Outer Layers**: HDI formed using laser drilled microvia, copper filled.
		Inner Layers: N* interconnected by a buried via, a mechanically drilled thru-hole, copper plated and polymer filled. * N is the number of inner layers.
i+N+i	HDI on 'i' number of outer layers where i >1.	**Outer Layers**: Greater than one HDI layer formed using laser drilled microvias*, copper filled. *Microvias can be stacked or staggered.
		Inner Layers: N* interconnected by a buried via, a mechanically drilled thru-hole, copper plated and polymer filled. * N is the number of inner layers.
ELIC	High-density routing on every layer.	**E**very **L**ayer **I**nterconnect **C**onnection: stacked microvias on every layer. The microvias are 100% copper filled.

Table 1: Typical stackup structures of HDI technology.

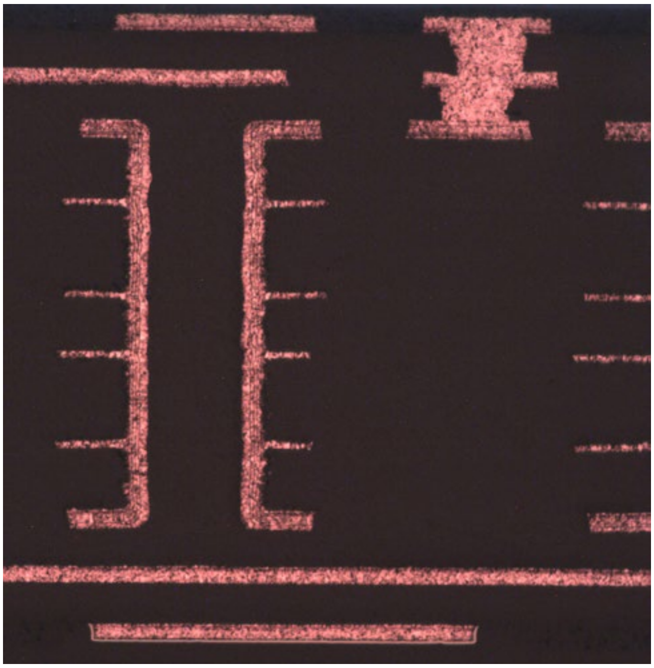


Figure 1: HDI: 2+N+2, stacked microvias, buried through-hole via.

in layers not requiring for routing in the design (Figure 4).

Multek has made extensive investments since 2004 in the invention and production scaling of customers' ELIC requirements, with

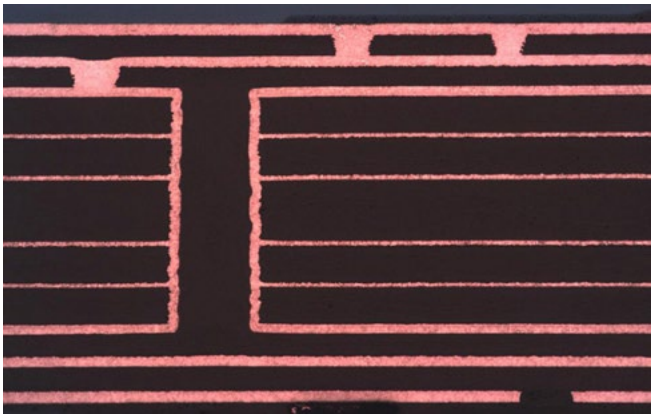


Figure 2: HDI: 2+N+2 staggered microvias, buried through-hole via.

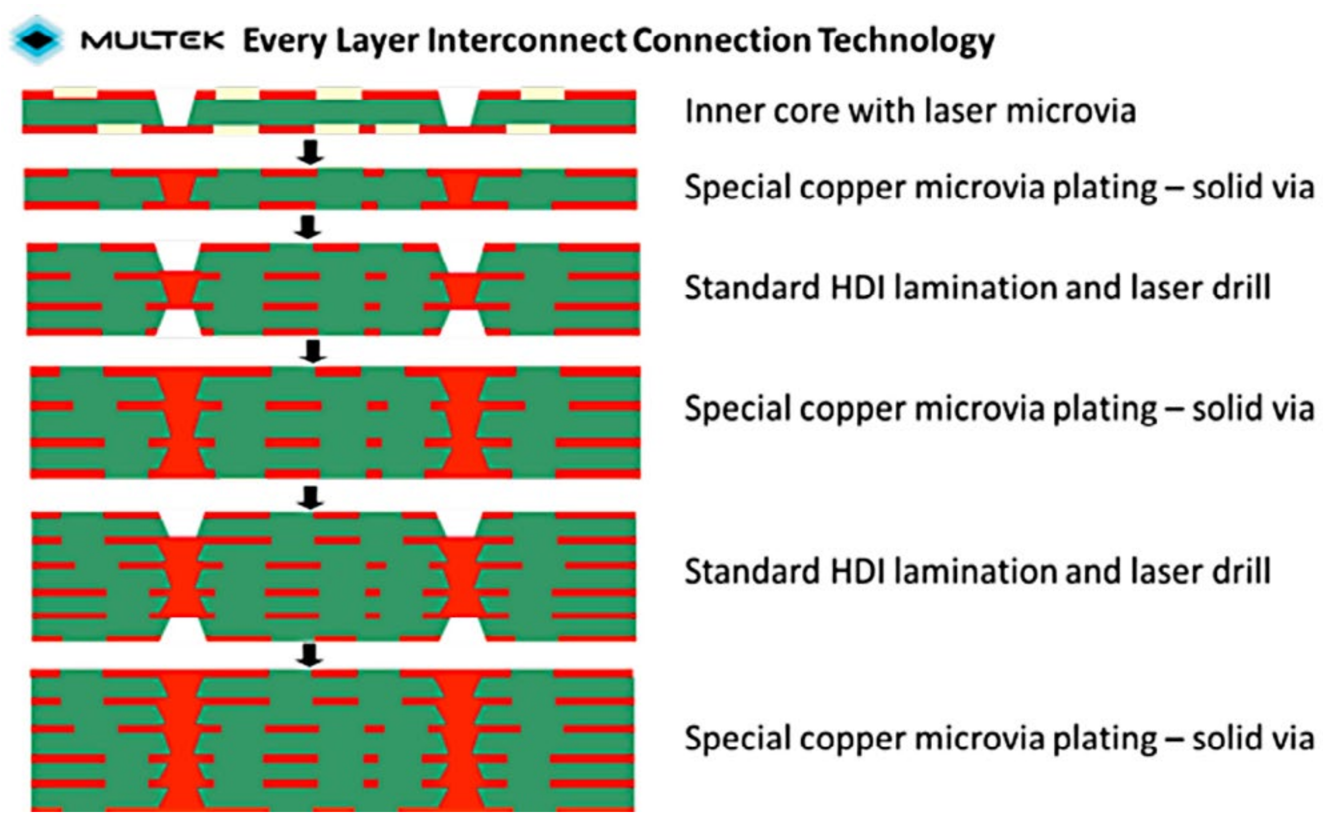


Figure 3: ELIC sequential lamination steps to form solid copper stacked microvias.

additional process engineering to implement core FPC processing into HDI rigid-flex designs now required by our customers with wearable and IoT circuit and module designs.

HDI: Enabling Technology for the Intelligence of Things

Flextronics has recognized that IoT is rapidly evolving to The Intelligence of Things to become a new ecosystem of smart, connected devices, machines and systems that interact to deliver greater capabilities, efficiencies, and experiences are changing the way we live, work and play. The innovation landscape driving The Intelligence of Things will increasingly propagate smart, connected products due to the adaptation of the core HDI interconnect platforms of rigid and flexible PCBs .

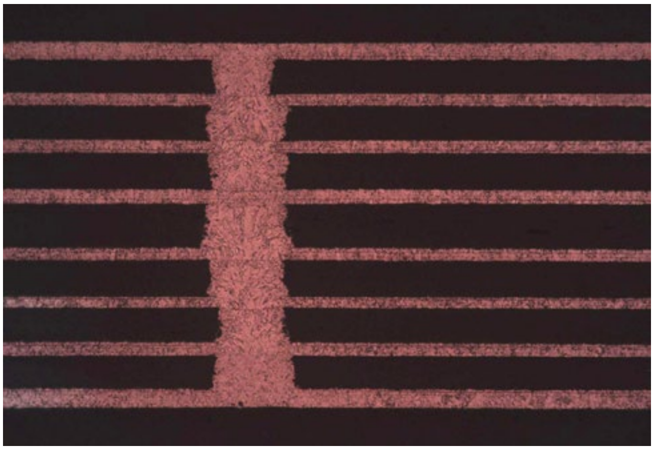
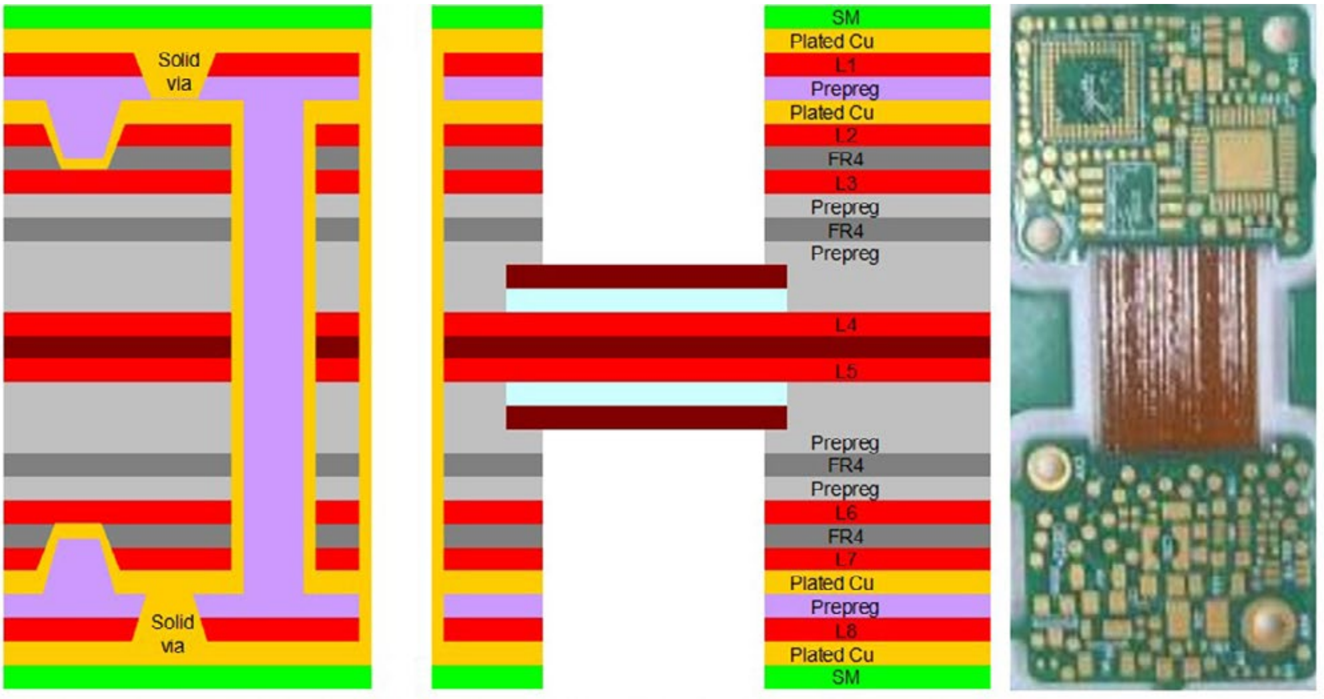


Figure 4: Every layer interconnect connection, 8-layer rigid.

Miniaturization:

HDI enabled the miniaturization of the printed circuit to address the demand for increasing functionality yet smaller form factors in mobile communication devices (i.e. cellphones and tablets). Another driving factor for HDI is increasing power requirements resulting from the additional functionality and also the growing size of the color display. These additional power requirements resulted in larger battery footprints. This accelerated the HDI adoption as the larger battery dimensions were expanding and the PCB size needed to shrink to accommodate the overall product outline. Early cellphone PCBs were X layer, standard thru-hole via technology and X mil lines and space



Figures 5: Stack-up of actual RFPCs using HDI technology in automotive application.

and average total thickness of 0.062 inches. Current mobile communication products such as Smart phones have HDI technology can be up to 14 layers, ELIC technology, 50 micron L/S inner layers, 37.5 micron L/S outer layers and total PCB thickness from 0.060 to 0.047 inches, based on core and pre-preg thickness options.

Smartphones presently have the functionality of a personal computing, high-resolution camera and video, transmission and receipt of data, and, yes, phone capabilities. The smartphone is now the hub of personal and device connection.

The HDI Building Blocks for Smart, Connected Products

HDI PCBs and HDI-FPC hybrid platforms are key building blocks in multiple applications across automotive, medical, data & storage, mobile communication and wearable technologies.

There are multiple benefits and advantage of HDI-RFPC hybrids that includes:

a) A single printed circuit with repeatable, reliable, high density interconnects.
b) System cost-saving resulting from component integration (eliminates connectors and other components).

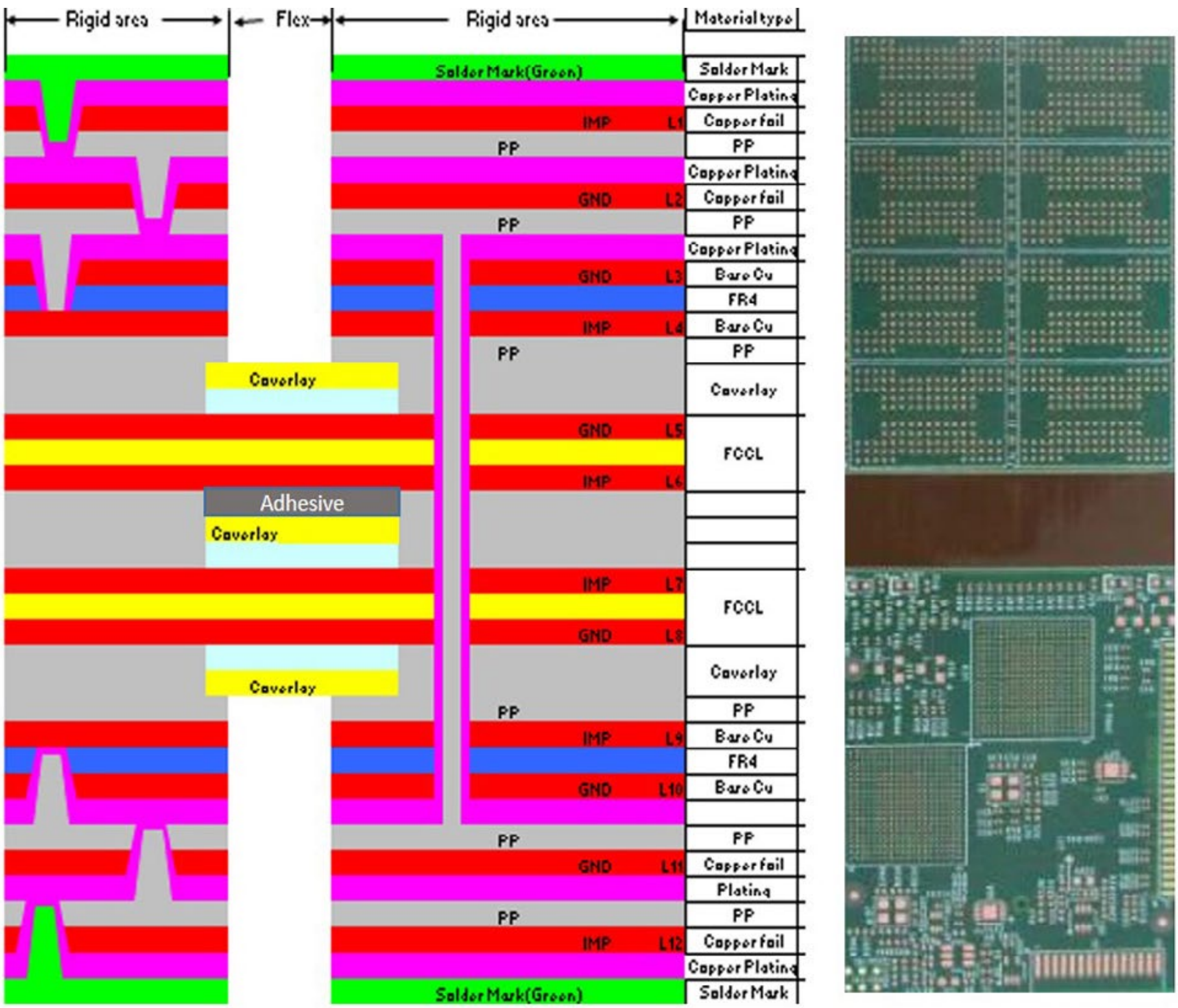


Figure 6: Stack-up of actual RFPCs using HDI technology in data storage application.

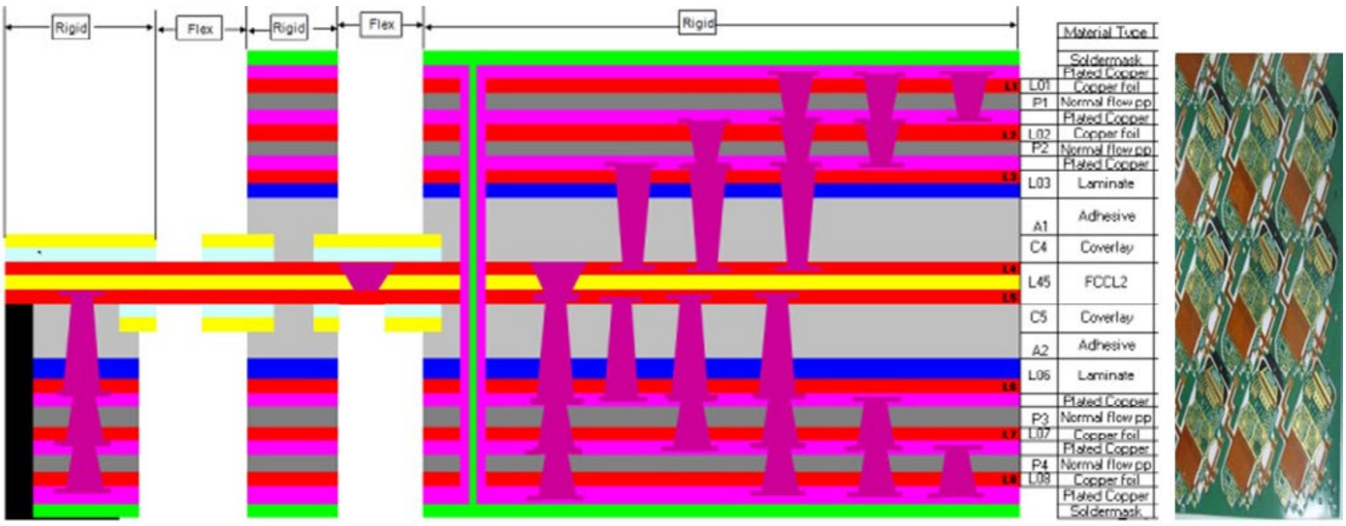


Figure 7: Stack-up of actual RFPCs using HDI technology in wearable technology application.

c) Elimination of wiring connections errors during installation and servicing, reduced assembly labor.
d) Three dimensional packaging where the flexible circuit can be bent to fit individual products to be installed in non-planar space.
e) Minimized weight and space, 75% less weight of conventional wiring type connection between multiple PCBs.
f) Improved reliability through elimination of connectors and reduced thermal stress on solder joints.
g) Thin, flat conductors and thin insulation resulting in improved thermal dissipation.
h) Greater electrical performance for consistent electrical impedance performance with integral ground planes.
i) Uniform electrical characteristics with consistent conductor spacing and insulation parameters.

Summary

From its inception, the printed circuit industry's success factors have been inventive response to new product designs' performance, reliability, and cost requirements. With the creation of the global cellular communications infrastructure over the last 20 years, Internet-enabled wireless communication and computing products have become an essential part of the fabric of life across the globe. Yet, this recent past is only a prologue to the major impact that the current expansion of the connectivity matrix between humans and smart devices and products will foretell. For example, the ELIC examples we have shown in this article took the global PCB industry a decade to evolve from early process concepts.

Industry leaders from all parts of the PCB supply chain must do more pre-competitive partnering to create and optimize the best solutions more quickly than in the past. At Multek, we expect that the rate of scaling of the next core processes, equipment, and materials envisioned for the massive deployment IoT designs must follow a more aggressive timeline of collaborative setting of new interconnect technology direction and investments. **PCB**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